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Question Paper Code : 57283

B.E/B.Tech. DEGREE EXAMINATION, MAY/JUNE 2016

Third Semester

Electronics and Communication Engineering

EC 6304 – ELECTRONIC CIRCUITS – I

(Regulations 2013)

Time : Three Hours

Maximum : 100 Marks

Answer ALL questions.

PART – A ($10 \times 2 = 20$ Marks)

1. What is an operating point ?
2. Give the methods of biasing a JFET.
3. What is the need of a load line ?
4. Draw a cascade amplifier and its ac equivalent circuit.
5. What is body effect in MOSFET ? How does it change the small-signal equivalent circuit of the MOSFET ?
6. Give the general conditions under which common source amplifier would be used.
7. A bipolar transistor has parameter $\beta_o = 150$, $C_\pi = 2$ pF, $C_\mu = 0.3$ pf and is biased at $I_{CQ} = 0.5$ mA. Determine the beta cut off frequency.
8. Sketch the expanded hybrid π model of the BJT.
9. What is a current mirror circuit ?
10. Sketch a MOSFET cascade current source and state its advantage.

PART – B (5 × 16 = 80 Marks)

11. (a) Compare the various methods of biasing using BJT in terms of their stability factors. **(16)**

OR

(b) With neat diagrams, explain two bias compensation techniques and state its advantages and disadvantages. **(16)**

12. (a) What are the changes in the a.c characteristics of a common emitter amplifier when an emitter resistor and an emitter bypass capacitor are incorporated in the design ? Explain with necessary equations. **(16)**

OR

(b) (i) Calculate the small signal voltage gain of an emitter follower circuit.

Given $\beta = 100$, $V_{BE(on)} = 0.7V$, $V_A = 80$ V, $I_{CQ} = 0.793$ mA, $V_{CEQ} = 3.4$ V. **(8)**

(ii) Draw and explain the operation of a darlington amplifier. **(8)**

13. (a) Design a JFET source follower circuit (Figure 13(a)) with a specified small signal voltage gain given $I_{DSS} = 12mA$, $V_p = -4V$, $\lambda = 0.01\ V^{-1}$. Determine R_s and I_{DQ} such that the small signal voltage gain is at least $A_v = V_o/V_i = 0.90$. **(16)**

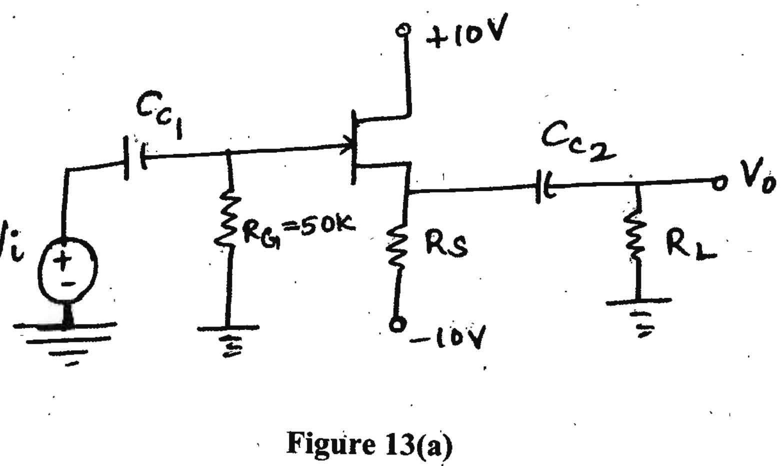

Figure 13(a)

OR

(b) Determine the small signal voltage gain of a common source circuit (Figure 13(b)) containing a source resistor. The transistor parameters are $V_{TN} = 0.8$ V, $Kn = 1$ mA/V^2 and $\lambda = 0$. **(16)**

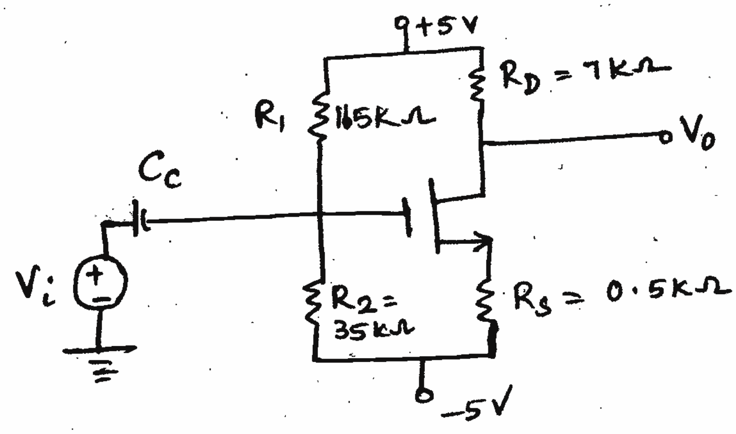

Figure 13(b)

14. (a) Determine the 3 dB frequencies and mid band gain of a cascade circuit. For the Figure 14(a) the parameters are $V^+ = 10$ V, $V = -10$ V, $R_s = 0.1$ kΩ, $R_1 = 42.5$ kΩ, $R_2 = 20.5$ kΩ, $R_3 = 28.3$ kΩ, $R_E = 5.4$ kΩ, $R_c = 5$ kΩ, $R_L = 10$ kΩ, $C_L = 0$. The transistor parameters are $\beta = 150$, $V_{BE(ON)} = 0.7$ V, $V_A = \infty$, $C_\pi = 35$ pF and $C_\mu = 4$ pF. **(16)**

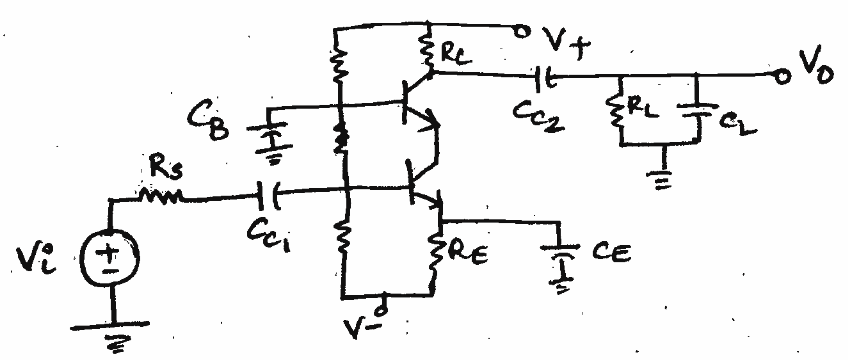

Figure 14(a)

OR

(b) The transistor in the figure. 14(b) has parameters $\beta = 125$, $V_{BE(ON)} = 0.7$ V, $V_A = 200$ V, $C_\pi = 24$ pF and $C_\mu = 3$ pF.

(i) Calculate the miller capacitor

(ii) Determine the upper 3 dB frequency

(iii) Determine the small signal mid band voltage gain **(16)**

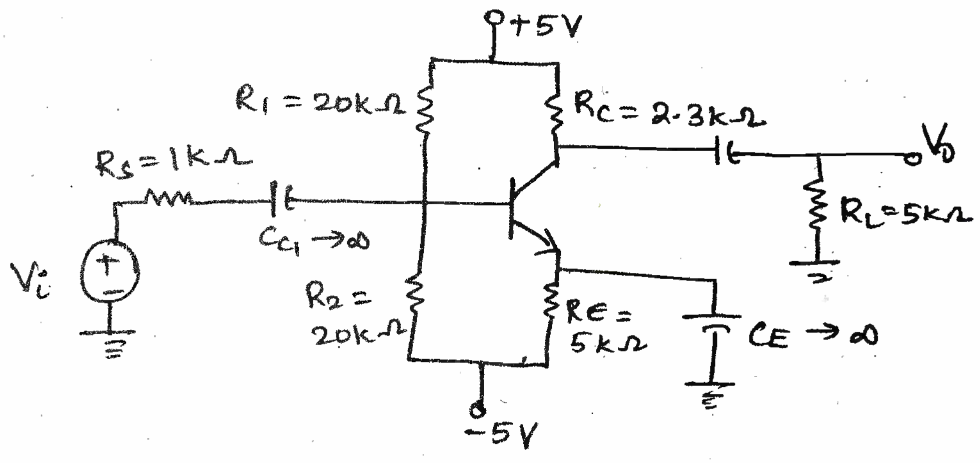

Figure. 14(b)

15. (a) For the circuit shown in the figure. 15(a) Let $V^+ = 10$ V, and $V^- = 0$ and the transistor parameters are $V_{TN} = 2$ V, $\frac{1}{2} \mu_n C_{ox} = 20\ \mu A/V^2$ and $\lambda = 0$. Design the circuit such that $I_{ref} = 0.5$ mA and $I_o = 0.2$ mA and M_2 remains biased in the saturation region for $V_{DS2} \geq 1$ V. **(16)**

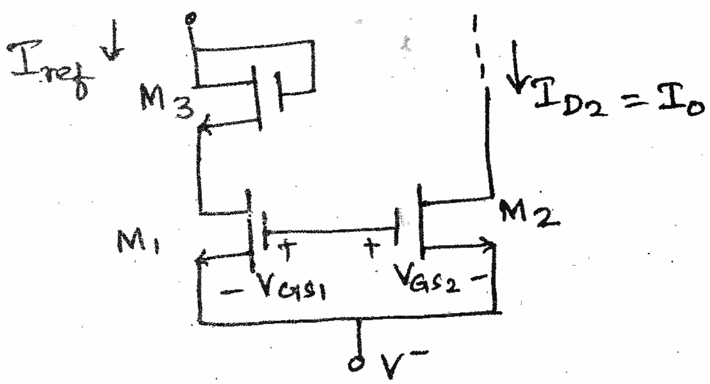

Figure 15(a)

OR

(b) With the necessary diagram explain about CMOS differential amplifier and derive the CMRR. **(16)**